Amendments to the Specification:

Please replace the paragraph beginning on page 11, line 2, with the following amended paragraph:

If, under normal operation, node **30** from comparator **21** is at logic 1, then node **32** is at logic 0. Node **30** is received at nFET **47** and pFET **42**, turning on the former and turning off the latter. Similarly, node **32** at logic zero will turn off nFET **44** and turn on pFET **46**. Using the example above, with node **36** originally set at logic 0, pFET **45** is turned on, while nFET **48** is turned off. Node **39** is set at logic 1, causing pFET **41** to be ~~tuned off~~ turned off and nFET **43** to be turned on. With the source of pFET **45** at supply voltage Vdd, and both pFETs **45** and **46** turned on, node **50** is brought to logic 1 state (Vdd). If a soft error is registered at node **36**, causing it to change to logic 1, then pFET **45** is turned off and nFET **48** is turned on. Similarly node **39** is switched to logic 0, causing pFET **41** to turn on and nFET **43** to turn off. With both nFETs **47** and **48** now turned on and nFET **48** source set at ground, node **50** is brought to logic 0. Thus, given that the inputs from comparator **21** do not change, a switch of state at node **36** and **39** (**36/39**) causes a switch at node **50**.

Please replace paragraph [0031] beginning on page 11 with the following amended paragraph:

One skilled in the art will notice that each fuse latch comparator performs the XOR circuit function as shown by the following: If input **30=39** (and therefore **32=36** and **30≠36** and **32≠39**) **50** is logic 1, because either **30=39**=logic 0 or **32=36**=logic 0. That is, if the gate inputs of the pFETs of pair **41/42** (corresponding to inputs **30/39**) are the same, then the inputs of the pFETs in pair **45/46** (corresponding to inputs **32/36**) must also be the same, and the inputs to nFETs in pair **47/48** (corresponding to inputs **30/36**), as well as those in pair **43/44** (corresponding to inputs **39/32** ~~inputs 30/32~~), must differ. Since either pFET pair **41/42** or **45/46** ~~30/39 or 32/36~~ is turned on, node **50** is connected to Vdd (logic 1), through the turned on pair.

Please replace paragraph [0032] on page 12 with the following amended paragraph:

If **30≠39** (and therefore **32≠36** and **30=36** and **32=39**), **50** is logic 0, because either **30=36**=logic 1 or **32=39**=logic 1. In other words, if the gate inputs to the pFETs of pair **41/42** (corresponding to inputs **30/39**) are different, then the gate inputs to pFETs in pair **45/46** (corresponding to inputs **32/36**) must also be different, and the inputs to nFETs in pair **47/48** (corresponding to inputs **30/36**), as well as those in pair **43/44** (corresponding to ~~inputs 30/32~~ inputs 39/32) must be the same. Whether pair **43/44** is turned on or **47/48** is turned on, node **50** is connected to ground (logic 0) through the turned on pair.

Please replace paragraph [0034] on beginning on page 12 with the following amended paragraph:

Figure 7 illustrates an exemplary embodiment of the present invention, particularly a method of detecting and correcting latch errors. After a radiation strike causes a latch soft error, a detector placed next to comparator **90** detects that the latch block parity bit **69** has flipped at step **702**, indicating a soft error in the latch block. In response, some type of signal processor is triggered. In one embodiment, a signal for reading out the errant fuse block is generated locally in the chip. After detecting the signal indicative of the parity bit error, at step **704**, a local message is sent to a signal generator with instructions to reset the latch block, once a trigger is received. At step **706**, the signal processor receives a trigger to generate a reset signal. At step **708**, the signal generator resets the latch block using ~~reset node 14~~ latch node 15 in latch **11**, shown in Figure 2. At this point, the latch may be reset to a default value, e.g. logic 1, by turning on load **14**. Next, in step **710**, fuse **12** is connected to latch node **15** by applying an appropriate voltage to the transistor at node **13**, which restores the proper state. If the fuse in question is not blown, the latch is flipped upon reread. This process occurs for each latch unit in the block, and results in all errant latches being reset to their respective correct fuse values. At the same time at

step **712**, a signal is sent through nFET **81** to restore parity bit latch **77**. Optionally, the stored parity bit **73** may then be reread in step **714** to establish that the parity bit and parity bit latch are restored to their correct settings, indicating that all the latches within the block are correctly set. For example, if the number of blown fuses in the block is odd, and after a soft error the number appears even, upon reread the parity bit and stored parity bit will again show an odd number of fuses blown.